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FACSIMILE TRANSMITTAL SHEET

TO: Examiner: Chuong D. NGO	FROM: Shawn W. O'Dowd
COMPANY: USPTO	DATE: May 8, 2006
FAX NUMBER: (571) 273-8300	TOTAL NO. OF PAGES INCLUDING COVER: 27
PHONE NUMBER:	SENDER'S REFERENCE NUMBER: Intel 2207/11272
RE: Application No.: 09/893,868	YOUR REFERENCE NUMBER: Group Art Unit: 2193

☐ URGENT ■ FOR REVIEW ☐ PLEASE COMMENT ☐ PLEASE REPLY ☐ CONFIRMATION

☐ ORIGINAL WILL FOLLOW ■ ORIGINAL WILL NOT FOLLOW

Notes/Comments:

APPEAL BRIEF

1. Fax Cover Sheet (1)
2. Fee Transmittal (and one copy) (2)
3. Petition for 3-month Extension of Time (1)
3. Appeal Brief (23)

Total: (27) pages

Certificate of Facsimile Transmittal

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Dated: May 8, 2006

Signature: Barbara Vance
Barbara Vance

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FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **1,520.00**

Complete if Known	
Application Number	09/893,868
Filing Date	June 29, 2001
First Named Inventor	Thomas D. FLETCHER
Examiner Name	Chuong D. NGO
Art Unit	2193
Attorney Docket No.	Intel 2207/11272

METHOD OF PAYMENT *(check all that apply)*

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	
				SUBTOTAL (1)	($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20 ** =		X	50.00	=	
Independent Claims		-3 *** =		X	200.00	=	
Multiple Dependent				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple dependent claim, if not paid
1204	200	2204	100	** Reissue independent claims over original patent
1205	50	2205	25	*** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	1,020
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	500	2452	250	Petition to revive – unavoidable	
1453	1,500	2453	750	Petition to revive – unintentional	
1501	1,400	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 1,520.00

SUBMITTED BY

Complete (if applicable)

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Signature	Lin Deng			*Date*	May 8, 2006

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Patent

Attorney Docket No.: 2207/11272
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	Thomas D. FLETCHER
SERIAL NO.	:	09/893,868
FILED	:	June 29, 2001
FOR	:	CASCADED DOMINO FOUR-TO-TWO REDUCER CIRCUIT AND METHOD
GROUP ART UNIT	:	2193
EXAMINER	:	Chuong D. NGO

VIA FACSIMILE

M/S: APPEAL BRIEF - PATENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING

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Dated: May 8, 2006 Signature Barbara Vance

Barbara Vance

ATTENTION: Board of Patent Appeals and Interferences

APPEAL BRIEF UNDER 37 CFR 41.37

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on December 7, 2005.

Application No.: 09/893,868
Date: May 8, 2006
APPEAL BRIEF – PATENT

1. REAL PARTY IN INTEREST

Intel Corporation is the real party in interest for all issues related to this application, (Recorded June 29, 2001, Reel/Frame: 011964/0168).

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings known to Appellant or Appellant's legal representative, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

3. STATUS OF THE CLAIMS

This application currently contains claims 1, 4-17, 19-25, 27-33, and 35-38. Claims 10-15, 21-25, 27-33 and 35-38 have been allowed. Claims 4 and 6-9 are objected to as being allowable if rewritten in independent form. Claims 1, 5, 16, 17, 19 and 20 have been rejected. Claims 1 and 5 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,340,388 to Earle ("Earle"). Claims 16, 17, 19, and 20 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,466,960 to Winters ("Winters").

4. STATUS OF AMENDMENTS

In its Response to the Final Office Action, Applicants amended claims 5, 13-16, 19-25, 27-30, 32-33, 35-38. These amendments were entered upon the filing of the Notice of Appeal. The attached listing of claims (section 8), reflects the current status of the claims.

5. SUMMARY OF THE INVENTION

Embodiments of the present invention provide topologies for cascaded domino four-to-two reducers. The present invention eliminates static CMOS stages in the four-to-two reducer by sequentially clocking the differential logic stages with a small delay between stages. In an embodiment, the delay between stages is approximately the delay of an inverter with a fanout of two, a delay which depends upon the process technology.

In the embodiment of claim 1, a first three-to-two reducer (*see, e.g.*, element 120 in Fig. 1) is provided, and a second three-to-two reducer (*see, e.g.*, element 150 in Fig. 1) is directly connected to the first three-to-two reducer. A first clock input (e.g., element 101 in Fig. 1) is connected to the first three-to-two reducer to receive a first clock signal. A second clock input (*e.g.*, element 102 in Fig. 1) is connected to the second three-to-two reducer to receive a second clock signal that is delayed from the first clock signal (*see, e.g.*, pg. 5, lines 13-15 and pg. 6, lines 3-21).

In the embodiment of claim 10 a circuit is provided including a first differential domino three-to-two reducer (*e.g.*, element 120 in Fig. 1) having three differential inputs and two differential outputs, wherein the first differential domino three-to-two reducer has an input to receive a first clock signal (*e.g.*, element 101 in Fig. 1). A second differential domino three-to-two reducer (*e.g.*, element 150 in Fig. 1) is provided having three differential inputs and two differential outputs, wherein one of the differential inputs of the second differential three-to-two reducer is connected to a differential output of the first differential three-to-two reducer, wherein the second differential domino three-to-two reducer has an input to receive a different clock signal (*see, e.g.*, pg. 5, lines 13-15 and pg. 6, lines 3-21).

In the embodiment of claim 16, a circuit is provided including a plurality of data inputs comprising three true inputs and three complement inputs (*see, e.g.*, pg. 4, lines 1-10). A differential exclusive-OR (XOR) gate (*e.g.*, element 130 in Fig. 1) is provided having six input ports each connected to one of the plurality of data inputs. A differential carry generate gate (*e.g.*, element 140 in Fig. 1) is provided having six input ports each connected to one of the plurality of data inputs, wherein the differential carry generate gate comprises a precharge block (*e.g.*, element 330 in Fig. 3), a first evaluation block (*e.g.*, element 350 in Fig. 3) connected to the three true inputs, and a second evaluation block (*e.g.*, element 360 in Fig. 3) connected to the three complement inputs. The first evaluation block and second evaluation block each have a plurality of transistors, wherein each of the transistors in the first evaluation block and second evaluation block are part of a transistor stack, and wherein the number of transistors in each of the stacks is the same (*see, e.g.*, page 10, line 9 to page 12, line 8).

In the embodiment of claim 21, a method is provided including a first operation of receiving three pair of true and complement data bits at a first differential domino three-to-two reducer (*see, e.g.*, element 201 in Fig. 2). Then, a first pair of true and complement sum bits are output from the first three-to-two reducer to a second differential domino three-to-two reducer during the evaluation phase of a first clock (*see, e.g.*, element 203 in Fig. 2). A fourth pair of true and complement data bits is received at the second differential domino reducer (*see, e.g.*, element 204 in Fig. 2). Also, a second pair of true and complement sum bits is output as well as a pair of true and complement carry output bits output during the evaluation phase of a second clock that is delayed from the first clock (*see, e.g.*, element 206 in Fig. 2 and pg. 5, lines 13-15 and pg. 9, line 4 to pg. 10, line 7).

In the embodiment of claim 25, a circuit is provided including a domino four-to-two reducer, wherein the four-to-two reducer includes a first three-to-two reducer (*e.g.*, element 120 in Fig. 1) that comprises a first logic gate, the first logic gate including a first evaluation block (*e.g.*, element 350 in Fig. 3) and a plurality of outputs, the first evaluation block including N-channel metal-oxide semiconductor transistors. A second three-to-two reducer (*e.g.*, element 150 in Fig. 1) that includes a second logic gate, the second logic gate including a second evaluation block (*e.g.*, element 360 in Fig. 3) and a plurality of inputs that are directly connected to the outputs of the first logic gate, the second evaluation block including N-channel metal-oxide semiconductor transistors. A first clock input (*e.g.*, element 101 in Fig. 1) is connected to the first three-to-two reducer to receive a first clock signal. A second clock input (*e.g.*, element 102 in Fig. 1) is connected to the second three-to-two reducer to receive a second clock signal that is delayed from the first clock signal (*see, e.g.*, pg. 5, lines 13-15 and pg. 10, line 9 to pg. 12, line 8).

In the embodiment of claim 33, a circuit is provided including a first differential domino three-to-two reducer (e.g., element 120 in Fig. 1) having three differential inputs and two differential outputs. A second differential domino three-to-two reducer (*e.g.*, element 150 in Fig. 1) is provided having three differential inputs and two differential outputs. One of the differential inputs of the second differential three-to-two reducer is connected to a differential output of the first differential three-to-two reducer, and wherein there are no static stages between the first and second differential domino three-to-two reducers, wherein the first differential domino three-to-two reducer has an input to receive a first clock signal and the

second differential domino three-to-two reducer has an input to receive a different clock signal (*see, e.g.*, pg. 5, lines 13-15; pg. 6, lines 3-21; and pg. 13, lines 13-18).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The rejection of claims 1 and 5 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,340,388 to Earle ("Earle").

B. The rejection of claims 16, 17, 19, and 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,466,960 to Winters ("Winters").

7. ARGUMENT

A. Legal Background

Under 35 U.S.C. §102(b), a claim is invalid if the invention claimed therein is described in a patent issuing more than one year prior to the filing of the subject patent application. Though a patent reference may have issued early enough (or filed early enough as the case for 35 U.S.C. §102(e)), that reference must also enable one skilled in the art to practice the claimed invention. *See* Akzo N.V. v. U.S. Int'l Trade Comm'n, 1 U.S.P.Q.2d (BNA) 1241, 1245 (Fed. Cir. 1986).

Absent anticipation it may be possible to combine two or more patents together to render a claimed invention obvious, and unpatentable, under 35 U.S.C. §103(a). In determining whether the claims are unpatentable it is necessary to look to what the references actually teach. "It is impermissible within the framework of §103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to

the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." In Re Wesslau, 147 U.S.P.Q. (BNA) 391, 393 (C.C.P.A. 1965). Accordingly, a prior art reference must be considered in its entirety, and portions thereof must be taken in proper context. MPEP § 2141.02; Bausch & Lomb, Inc. v. Barnes-Hind, Inc., 230 U.S.P.Q. (BNA) 416, 419 (Fed. Cir. 1986).

B. Claims 1 and 5 are not anticipated by Earle

Claims 1 and 5 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,340,388 to Earle. Looking at claim 1, this claim recites among other features, first and second clock inputs where the second clock signal is delayed from the first clock signal. Such a feature is not shown in Fig. 2 of Earle in that the same clock signal is provided to each of the carry save adders (CSAs). In other words, the clock signal on line 42 in Fig. 2 is the same clock signal, though inverted, from the clock signal on line 32. No delay is shown or suggested by the Earle reference. Since a feature of the claims is missing from the Earle reference, the rejection of claims 1 and 5 (which depends from and further defines claim 1) under 35 U.S.C. §102(b) is in error.

C. Claims 16, 17, 19 and 20 are not anticipated by Winters

Claim 16 recites a differential carry generate gate that has a first evaluation block and a second evaluation block that each have a plurality of transistors, "wherein each of the transistors in the first evaluation block and second evaluation block are part of a transistor stack, and wherein the number of transistors in each of said stacks is the same."

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Applicant submits that neither Winters nor any art of record disclose or suggest "wherein each of the transistors in the first evaluation block and second evaluation block are part of a transistor stack, and wherein the number of transistors in each of said stacks is the same." To the contrary, the circuit shown in FIG. 3A of Winters, which the Examiner relies upon in rejecting claim 16, does not meet these limitations. This circuit contains five transistors 25 in a first block and five transistors 26 in a second block. Although each block does contain two stacks with two transistors in each block, each block also contains a single transistor (connected to BH and BL) that is not stacked with any other transistors. Thus, the circuit in FIG. 3A of Winters does not meet the limitation "wherein each of the transistors in the first evaluation block and second evaluation block are part of a transistor stack, and wherein the number of transistors in each of said stacks is the same" of claim 16.

Applicant also notes that there is no evidence of a motivation to modify the prior art references to obtain the claimed invention. *See, e.g.*, In re Zurko, 258 F.3d 1379, 1368 (Fed. Cir. 2001) (holding that an Examiner must "point to some concrete evidence in the record" of a motivation to combine or modify the references to support an obviousness rejection).

In the Final Office Action, it is asserted that there are obvious errors in Fig. 3A of Winters. Applicant submits that the description at Col. 5, lines 18-55 and Fig. 3A are so replete with such alleged "errors" that it cannot be used properly for this rejection. Looking at Col. 5, lines 34-41, Winters describes the circuit of Fig. 3A to be used to perform the logic function of equation 8 (i.e., A XOR B XOR Cin; see Col.2, line 23). Given Fig. 3A and the description provided in Winters, one skilled in the art would not be led to the claimed invention. The changes that the Examiner is suggesting for the drawing of Fig. 3A of Winters are excessive.

First, the equation alluded to in the Office Action (AB+AB+BC) appears nowhere in Winters. Second, one of the "25" transistors is to be connected in a way different from that shown in the drawing. Third, one of the "26" transistors is to be connected in a way different from that shown in the drawing. Fourth, one of the gate inputs from one of the "26" transistors is to be changed. Applicant submits that the Office Action is impermissively relying on the description of the present application to allegedly correct errors in a drawing that are described to implement a completely different function.

The Advisory Action provides a marked-up version of Fig. 3A of Winters. Though the Advisory Action concludes that the Fig. 3A can be "simply" corrected, Applicant contends the opposite as detailed above. For at least these reasons, the rejection of claim 16 (and claims 17, 19 and 20, which depend therefrom) is believed to be in error.

D. CONCLUSION

Appellant respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1 and 5 under 35 U.S.C. § 102(b) and claims 16, 17, 19, and 20 under 35 U.S.C. § 102(e) and direct the Examiner to pass the case to issue.

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The Commissioner is hereby authorized to charge the appeal brief fee of $500.00 and any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. 11-0600. A copy of this sheet is enclosed for that purpose.

Respectfully submitted,

Date: May 8, 2006

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Application No.: 09/893,868
Date: May 8, 2006
APPEAL BRIEF – PATENT

APPENDIX

(Brief of Appellant Thomas D. Fletcher
U.S. Patent Application Serial No. 09/893,868)

8. CLAIMS ON APPEAL

The claims in their current form (including those claims under appeal) are presented below:

1. A circuit comprising

a first three-to-two reducer;

a second three-to-two reducer directly connected to the first three-to-two reducer;

a first clock input connected to the first three-to-two reducer to receive a first clock signal; and

a second clock input connected to the second three-to-two reducer to receive a second clock signal that is delayed from the first clock signal.

2-3. (Cancelled).

4. The circuit of claim 1, wherein the delay between the first clock signal and the second clock signal is approximately the delay of an inverter with a fanout of 2.

5. The circuit of claim 1, wherein the circuit further comprises two set-reset latches to convert the outputs of the second three-to-two reducer to static logic.

6. The circuit of claim 1, wherein the first and second three-to-two reducer both comprise a symmetric carry generate gate.

7. The circuit of claim 6, wherein the symmetric carry generate gates have a first evaluation block of transistors and a second evaluation block of transistors, wherein the first evaluation block and second evaluation block each have the same number of transistors.

8. The circuit of claim 7, wherein the symmetric carry generate gates have six data inputs, and wherein the gate of each of the transistors in both the first evaluation block and the second evaluation block is connected to one of the six data inputs.

9. The circuit of claim 6, wherein the first evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, wherein the second evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, and wherein the second evaluation

block has the same number of transistors in said parallel relationship as the first evaluation block and the same number of transistors in said serial relationship as the first evaluation block.

10. A circuit comprising:

a first differential domino three-to-two reducer having three differential inputs and two differential outputs, wherein the first differential domino three-to-two reducer has an input to receive a first clock signal; and

a second differential domino three-to-two reducer having three differential inputs and two differential outputs, wherein one of the differential inputs of the second differential three-to-two reducer is connected to a differential output of the first differential three-to-two reducer, wherein the second differential domino three-to-two reducer has an input to receive a different clock signal.

11. The circuit of claim 10, wherein there are no static stages between the first and second differential domino three-to-two reducers.

12. The circuit of claim 10, wherein the first differential three-to-two reducer comprises:

a differential exclusive-OR (XOR) gate having three differential inputs and a differential output; and

a differential carry generate gate having three differential inputs and a differential output.

13. The circuit of claim 12, wherein the three differential inputs to the carry generate gate comprise three true inputs and three complement inputs, and wherein the Miller coupling for the true inputs is equal to the Miller coupling for the complement inputs.

14. The circuit of claim 13, wherein the differential output of the carry generate gate comprises a true output and a complement output, and wherein the output drive strength for the true output is the same as the output drive strength for the complement output.

15. The circuit of claim 12, wherein the load for the true inputs to the carry generate gate is the same as the load for the complement inputs, wherein the pull down strength for the true output is the same as the pull down strength for the complement output, and wherein the pull down strength for the true inputs is the same as the pull down strength for the complement inputs.

16. A circuit comprising:

a plurality of data inputs comprising three true inputs and three complement inputs;

a differential exclusive-OR (XOR) gate having six input ports each connected to one of said plurality of data inputs; and

a differential carry generate gate having six input ports each connected to one of said plurality of data inputs, wherein said differential carry generate gate comprises a precharge

block, a first evaluation block connected to said three true inputs, and a second evaluation block connected to said three complement inputs, wherein the first evaluation block and second evaluation block each have a plurality of transistors, wherein each of the transistors in the first evaluation block and second evaluation block are part of a transistor stack, and wherein the number of transistors in each of said stacks is the same.

17. The circuit of claim 16, wherein the carry generate gate includes a first transistor connected to ground to provide a path to ground.

18. (Cancelled).

19. The circuit of claim 17, wherein the carry generate gate has a true output and a complement output, wherein the three true inputs comprise a first true input, a second true input, and a third true input, wherein the three complement inputs comprise a first complement input, a second complement input, and a third complement input, and wherein the first evaluation block comprises:

a second transistor and third transistor each having a drain connected to the first transistor and a gate connected to the first true input;

a fourth transistor having a drain connected to the first transistor and a gate connected to the second true input;

a fifth transistor having a drain connected to a source of the second transistor, a gate connected to the second true input, and a drain connected to the complement output; and

a sixth transistor having a drain connected to a source of the fourth transistor, a gate connected to the third true input, and a source connected to the complement output.

20. The circuit of claim 19, further comprising:

a seventh transistor and eighth transistor each having a drain connected to the first transistor and a gate connected to the first complement input;

a ninth transistor having a drain connected to the first transistor and a gate connected to the second complement input;

a tenth transistor having a drain connected to a source of the seventh transistor, a gate connected to the second complement input, and a drain connected to the true output; and

an eleventh transistor having a drain connected to a source of the ninth transistor, a gate connected to the third complement input, and a source connected to the true output.

21. A method comprising:

receiving three pair of true and complement data bits at a first differential domino three-to-two reducer;

outputing a first pair of true and complement sum bits from the first three-to-two reducer to a second differential domino three-to-two reducer during the evaluation phase of a first clock;

receiving a fourth pair of true and complement data bits at the second differential domino reducer; and

outputting a second pair of true and complement sum bits and a pair of true and complement carry output bits output during the evaluation phase of a second clock that is delayed from the first clock.

22. The method of claim 21, wherein the first pair of true and complement sum bits are outputted directly to the second three-to-two reducer from the first three-to-two reducer.

23. The method of claim 22, wherein providing the first true and complement sum bits to the second three-to-two reducer comprises:

outputting the first true and complement sum bits to an exclusive-or (XOR) gate; and

outputting the first true and complement sum bits to a symmetric carry generate gate.

24. The method of claim 21, wherein the method further comprises:

receiving the second true and complement sum bits at a first latch;

outputting a true sum output from the first latch;

receiving the true and complement carry output bits at a second latch; and

outputting a complement sum output from the second latch.

25. A circuit comprising a domino four-to-two reducer, wherein the four-to-two reducer comprises:

a first three-to-two reducer that comprises a first logic gate, the first logic gate comprising a first evaluation block and a plurality of outputs, the first evaluation block comprising N-channel metal-oxide semiconductor transistors;

a second three-to-two reducer that comprises a second logic gate, the second logic gate comprising a second evaluation block and a plurality of inputs that are directly connected to the outputs of the first logic gate, the second evaluation block comprising N-channel metal-oxide semiconductor transistors;

a first clock input connected to the first three-to-two reducer to receive a first clock signal; and

a second clock input connected to the second three-to-two reducer to receive a second clock signal that is delayed from the first clock signal.

26. (Cancelled)

27. The circuit of claim 25, wherein the delay between the first clock signal and the second clock signal is approximately the delay of an inverter with a fanout of 2.

28. The circuit of claim 25, wherein the four-to-two reducer further comprises two set-reset latches to convert the outputs of the second three-to-two reducer to static logic.

29. The circuit of claim 25, wherein the first evaluation block and second evaluation block each have the same number of transistors.

30. The circuit of claim 25, wherein the first logic gate and second logic gate are both symmetric carry generate gates.

31. The circuit of claim 30, wherein the symmetric carry generate gates have six data inputs, and wherein the gate of each of the transistors in both the first evaluation block and the second evaluation block is connected to one of the six data inputs.

32. The circuit of claim 25, wherein the first evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, wherein the second evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, and wherein the second evaluation block has the same number of transistors in said parallel relationship as the first evaluation block and the same number of transistors in said serial relationship as the first evaluation block.

33. A circuit comprising:

a first differential domino three-to-two reducer having three differential inputs and two differential outputs; and

a second differential domino three-to-two reducer having three differential inputs and two differential outputs, wherein one of the differential inputs of the second differential three-to-two reducer is connected to a differential output of the first differential three-to-two reducer, and wherein there are no static stages between the first and second differential domino three-to-two reducers, wherein the first differential domino three-to-two reducer has an input to receive a first clock signal and the second differential domino three-to-two reducer has an input to receive a different clock signal.

34. (Cancelled).

35. The circuit of claim 33, wherein the first differential three-to-two reducer comprises:

a differential exclusive-OR (XOR) gate having three differential inputs and a differential output; and

a differential carry generate gate having three differential inputs and a differential output.

36. The circuit of claim 35, wherein the three differential inputs to the carry generate gate comprise three true inputs and three complement inputs, and wherein the Miller coupling for the true inputs is equal to the Miller coupling for the complement inputs.

37. The circuit of claim 36, wherein the differential output of the carry generate gate comprises a true output and a complement output, and wherein the output drive strength for the true output is the same as the output drive strength for the complement output.

38. The circuit of claim 35, wherein the load for the true inputs to the carry generate gate is the same as the load for the complement inputs, wherein the pull down strength for the true output is the same as the pull down strength for the complement output, and wherein the pull down strength for the true inputs is the same as the pull down strength for the complement inputs.

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9. EVIDENCE APPENDIX

No further evidence has been submitted with this Appeal Brief.

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10. RELATED PROCEEDINGS APPENDIX

Per Section 2 above, there are no related proceedings to the present Appeal.